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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/055,266	01/22/2002	Ki-won Choi	9898-208	6747

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EXAMINER

NADAV, ORI

ART UNIT	PAPER NUMBER
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2811

DATE MAILED: 10/12/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/055,266	Applicant(s) CHOI, KI-WON	
	Examiner Ori Nadav	Art Unit 2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 05 August 2005.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-10, 12-16, 26 and 27 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-10, 12-16, 26 and 27 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 1-4, 6-10, 12-16, 26 and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admitted Prior Art (AAPA) in view of Smith (6,707,149).

It should be pointed out that in the following rejection, the adjectives "added", "redundant" and "normal" do not structurally or functionally distinguish one similar element from another.

Regarding claims 1, 13 and 26, AAPA teaches in figures 1-3 and related text a semiconductor package comprising:

a substrate (10) including a redundant bond finger (the 3rd bond finger [2] from the right side of the figure 3), an added bond finger (the 6th bond finger [2] from the right side of the figure 3) connected to a redundant solder ball pad 22 (the second solder ball from the right);

a semiconductor chip (6) having an added bond pad (15) attached to the substrate (10);

a normal wire bonding unit (4) coupled between the added bond pad (15) and the redundant bond finger (the 3rd bond finger [2] from the right side of the figure 3).

AAPA does not teach an added wire bonding unit coupled between the redundant bond finger and the added bond finger.

Smith teaches in figure 5b and related text a wire coupled between two pads (or bond finger) (36). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Smith into the device taught by AAPA in order to increase the number of interconnection between the substrate and the other device. The combined device shows an added wire bonding unit coupled between the redundant bond finger and the added bond finger; wherein the added bond pad is electrically connected to the redundant solder ball pad via the redundant bond finger and the added bond finger.

The claimed limitations of “added bond finger”, “added bond pad” and “added wire bonding unit”, are process limitations and would not carry patentable weight in this claim drawn to a structure, because distinct structure is not necessarily produced.

Note that a “product by process” claim is directed to the product per se, no matter how actually made, *In re Hirao*, 190 USPQ 15 at 17 (footnote 3). See also *In re Brown*, 173 USPQ 685; *In re Luck*, 177 USPQ 523; *In re Fessmann*, 180 USPQ 324; *In re Avery*, 186 USPQ 161; *In re Wertheim*, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); and *In re Marosi et al.*, 218 USPQ 289, all of which make it clear that it is the patentability of the final product per se which must be determined in a “product by process” claim, and not the patentability of the process, and that an old or obvious

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product produced by a new method is not patentable as a product, whether claimed in “product by process” claims or not. Note that the applicant has the burden of proof in such cases, as the above case law makes clear.

Regarding claims 2 and 14, the combined device shows an encapsulant (AAPA; 7) for encapsulating the semiconductor chip, the normal and added wire bonding units.

Regarding claims 3 and 15, the combined device shows a solder ball (AAPA; 13) connected to the redundant solder ball pad.

Regarding claim 4, the combined device teaches the substrate (AAPA; 10) is a single layer substrate on which a printed circuit pattern (AAPA; 14) is formed.

Regarding claim 6, the combined device shows a solder mask is not formed on the added bond finger (AAPA; the 6th bond finger [2] from the right side of the figure 3).

Regarding claim 7, the combined device shows the added wire bonding unit (Smith; wire) is formed over the substrate (Smith; 28).

Regarding claim 8, the combined device shows the added wire bonding unit (Smith; wire) is formed on an outer region of the substrate (Smith; 28) on which the semiconductor chip (Smith; 38) is mounted.

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Regarding claim 9, the combined device shows the added wire bonding unit (Smith; wire) is one unit.

Regarding claim 10, the combined device shows the semiconductor chip (Smith; 38) is attached to the substrate (Smith; 28) using an adhesive (Smith; 26).

Regarding claim 12, the combined device shows the added bond finger (AAPA; the 6th bond finger [2] from the right side of the figure 3) has the same pad shape as that of the redundant bond finger (AAPA; the 3rd bond finger [2] from the right side of the figure 3).

Regarding claim 16, the combined device shows the first printed circuit pattern (AAPA; 14) and a second printed circuit pattern (AAPA; 14') each have a width that enables wire bonding to be performed thereon.

Regarding claim 27, the combined device shows the added bond finger (AAPA; the 6th bond finger [2] from the right side of the figure 3) is not directly connected to the added bond pad.

3. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA in view of Smith, as applied to claim 1 above, and further in view of Sota et al. (6,064,111). AAPA and Smith teach substantially the entire claimed structure, as applied to claim 1 above, except a substrate is a double layer substrate.

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Sota et al. teach the double layer substrate (column 7, lines 17-20).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Sota et al. into the device taught by AAPA and Smith in order to improve the interchangeability of the semiconductor device in the double layer substrate.

Response to Arguments

Applicant argues that the 6th bond finger from the right side of figure 3 of AAPA's device is not an added bond finger, because this bond finger is an existing bond finger.

Applicant claims a final structure of a semiconductor package. The claimed limitations of "added bond finger", "added bond pad" and "added wire bonding unit", are process limitations since these elements have been added during the process of making the final structure of the claimed semiconductor package.

Applicant argues that nothing is connected to redundant solder ball pad 22 of figure 3 of AAPA's device.

Redundant solder ball 22 is taken to be the second solder ball from the right. This solder ball is clearly connected to the 6th bond finger by wiring 14. Therefore, the added bond finger is connected to the redundant solder ball pad, as claimed.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ori Nadav whose telephone number is 571-272-1660. The examiner can normally be reached between the hours of 7 AM to 4 PM (Eastern Standard Time) Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Stephen Loke can be reached on 571-272-1657. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

A handwritten signature in black ink, appearing to read 'Ori Nadav', is positioned above the printed name.

O.N.
10/11/05

ORI NADAV
PRIMARY EXAMINER
TECHNOLOGY CENTER 2800